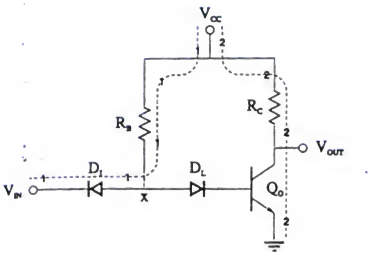
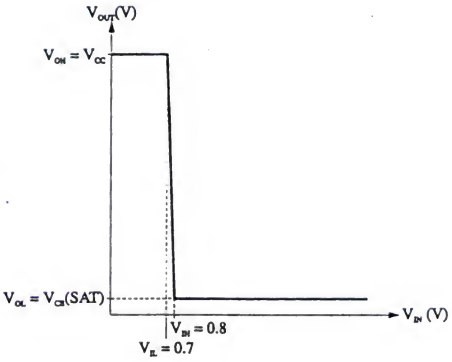
Chapter 6 - Diode Transistor Logic - DTL

Basic DTL Inverter

* This family of logic circuits was introduced to overcome the low fan-out of RTL for $V_{out} = V_{OH}$





Output high voltage $\equiv V_{OH}$

* For V_{IN} low D_I is forward biased

$$V_X = V_{IN} + V_{D,I}(ON) < V_{D,L}(ON) + V_{BE,Q}(FA)$$

Thus not large enough to turn on D_L & Q_0 therefore Q_0 is cutoff and $I_{RC} = I_C = 0$

$$V_{out} = V_{CC} - I_{RC} R_C = V_{CC} = V_{OH}$$

Input low Voltage $\equiv V_{IL}$

* Increasing V_{IN} to the point where Q_0 just turns on is achieved when

$$V_{IN} = V_{BE}(FA) = V_{IL}$$

Output low voltage $\equiv V_{OL}$

* Increasing V_{IN} (and therefore V_X) further eventually drives Q_0 into saturation giving

$$V_{out} = V_{CE,Q}(sat) = V_{OL}$$

Input High Voltage $\equiv V_{IH}$

Transistor Q_0 enters saturation at

$$V_{IN} = V_{BE,Q}(sat) + V_{D,L}(ON) - V_{D,I}(ON) = V_{BE}(sat) = V_{IH}$$

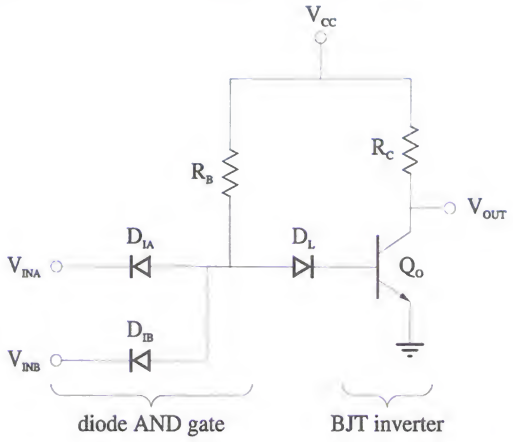
* Resistor R_B must be chosen small enough such that Q_o is in saturation when

$$V_x = V_{BE(sat)} + V_{D(ON)}$$

* Since V_{IL} & V_{IH} differ only by $V_{BE(sat)} - V_{BE(FA)}$ the transition width between output high & low logic states is quite abrupt

Basic DTL NAND Gate

* Addition of another input diode resembles a diode AND gate connected to a BJT inverter.



Modified DTL

Additional Level-Shifting.

* An additional level shifting diode D_{L2} has been added in series with D_L to shift the logic level transition by $V_{D(ON)}$ on the VTC input voltage axis this improves the low noise margin NM_L while still exhibiting an acceptable high noise margin NM_H

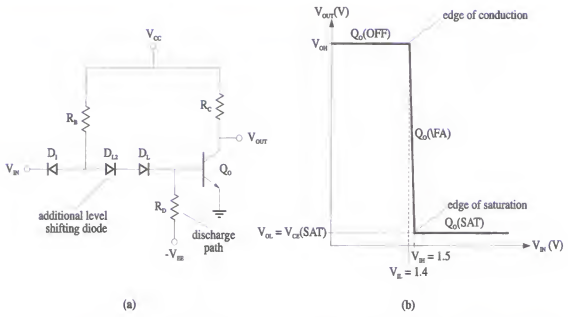


FIGURE 6.3 Modified DTL: (a) Circuit with additional level-shifting diode and discharge path, (b) Voltage transfer characteristic

* The additional level-shifting diode also avoids the problem of Q_o turning on before V_{IN} reaches 0.7V.

* The addition of D_{L2} increases V_{IL} & V_{IH} by $V_{D(ON)} = 0.7V$

Discharge Path

* R_D & $-V_{EE}$ at the base of Q_o provide a path for discharge of the stored base charge of Q_o when switched from saturation to cutoff

* The need for an additional source voltage can be avoided by simply taking $-V_{EE}$ to be ground and using a smaller valued resistance for R_D.

Transistor Modified DTL

* The fan-out of DTL circuits can be further improved by replacing the level-shifting diode D_{L2} with a BJT Q_L & splitting R_B into two resistors ρR_B & $(1-\rho)R_B$, whose sum is R_B

* This circuit improves fan-out by Q_L providing more base-driving current to Q_O allowing Q_O to sink more current from an output load.

* If $\rho = 1$ the J_{BC} of Q_L is shorted causing Q_L to act as a diode.

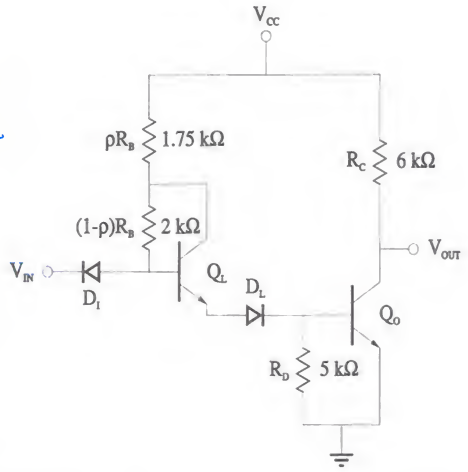


FIGURE 6.4 Transistor Modified DTL (930 Series)

TABLE 6.1 Purpose of DTL Elements

Element	Purpose
D_I	Input diode, limits I_{IH}, and provides ANDing
ρR_B	Limits I_{IL}
$(1-\rho)R_B$	Self biases Q_L
Q_L	Base-emitter level-shifting for shift of transition width and provides base driving current to Q_O
D_L	Level-shifting diode for shift of transition width
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_O	Output inverting BJT and output low driver for current sinking pull-down
R_C	Passive current sourcing pull-up

TABLE 6.2 State of Diodes and BJTs for Output High and Low Levels

Element	V_{OH}	V_{OL}
D_I	On	Cutoff
Q_L	Cutoff	Forward active
D_L	Cutoff	On
Q_O	Cutoff	Saturated

Example 6.1 *VTC of Transistor Modified DTL*

Determine the VTC of the transistor modified DTL inverter in Figure 6.4. Use $V_D(ON) = 0.7$ V for the diodes and $V_{BE}(FA) = 0.7$ V, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ V for the BJTs.

$V_{OH} = V_{CC} = 5V$

$V_{OL} = V_{CE,O}(sat) = 0.2V$

Q_O turns on at

$V_{IL} = V_{BE,O}(FA) + V_{D,L}(ON) + V_{BE,L}(FA) - V_{D,I}(ON)$

$= 2V_{BE}(FA) = 2(0.7) = 1.4V$

and saturates at $V_{IH} = V_{BE,O}(sat) + V_{D,L}(ON) + V_{BE,L}(FA) - V_{D,I}(ON)$

$V_{IH} = V_{BE}(sat) + V_{BE}(FA) = 0.8 + 0.7 = 1.5\ V$

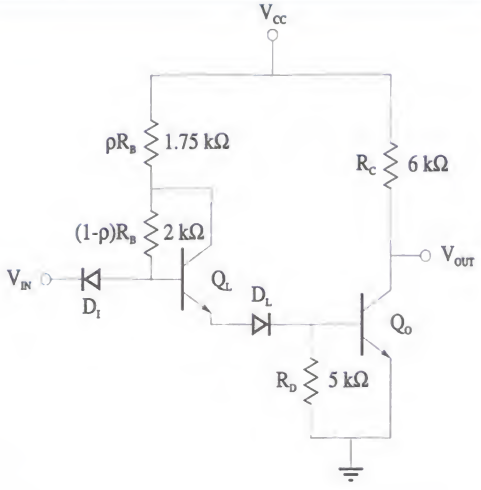


FIGURE 6.4 Transistor Modified DTL (930 Series)

* Note that Q_L can never saturate because the voltage polarity for the resistor $(1-\rho)R_B$ maintains a negative $V_{BC,L}$ for Q_L.

DTL NAND Gate

* For any input low

$$V_x = V_{IN}(low) + V_{D,1}(ON)$$
$$< V_{BE,L}(FA) + V_{D,L}(ON) + V_{BE,O}(FA)$$

$\therefore Q_O$ is cutoff

$$V_{out} = V_{OH} = V_{CC}$$

* for all inputs high

V_x is high allowing Q_O to saturate (provided that ρR_B is chosen properly)

$$V_{out} = V_{CE,O}(Sat) = V_{OL}$$

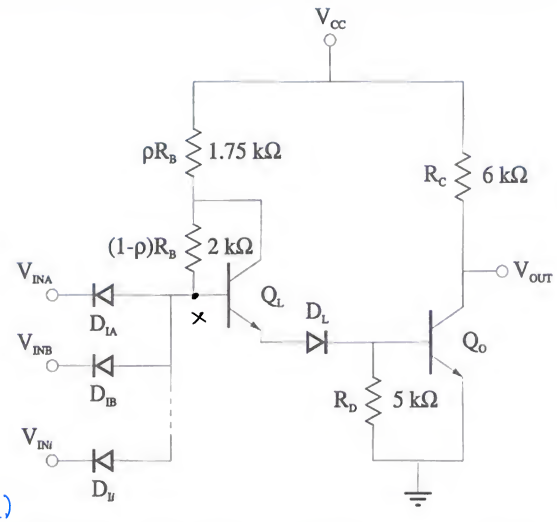


FIGURE 6.5 930 Series DTL NAND Gate

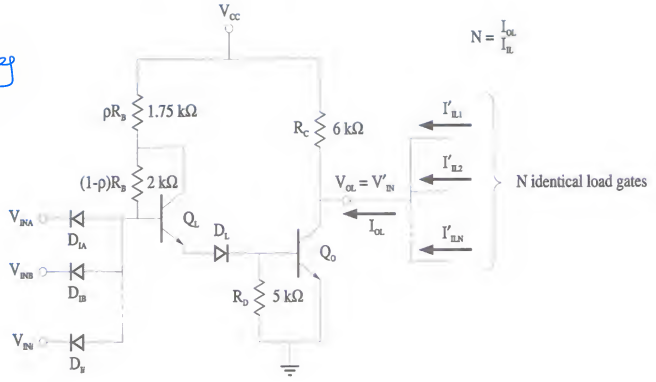
therefore:

The DTL logic family provides the logical NAND operation

DTL Fan-out

* when $V_{out} = V_{OH}$ for the driving gate reverse biases the input diodes of all load gates. such gates sink very little current & hence do not impose a fan-out restriction.

* The maximum fan-out is obtained by determining how much output current I_{OL} the driving gate can sink from multiple identical output gates



$$N I_{IL} = I_{OL}$$

$$N = \frac{I_{OL}}{I_{IL}}$$

* To determine N we use the following figure. which shows one of the load gate explicity with $V_{out} = V_{IN} = V_{OL}$

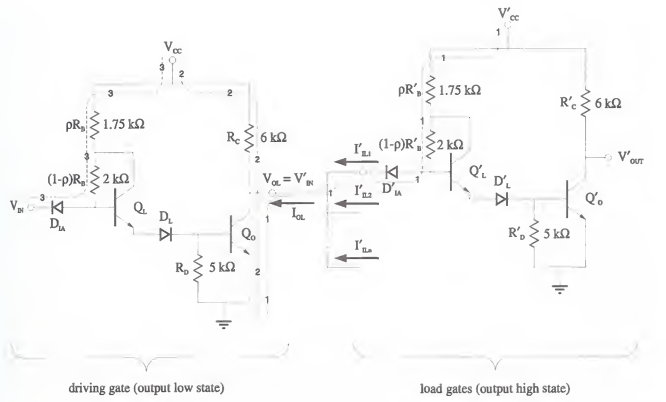


FIGURE 6.7 Cascaded DTL Gates for Fan-out and Power Dissipation Calculation

Input low current $\equiv I_{IL}$

$$I'_{\rho RB} = I_{IL} = \frac{V_{CC} - V'_{D,(ON)} - V_{CE,O(sat)}}{\rho R'_B + (1-\rho) R'_B}$$

$$= \frac{V_{CC} - V_{D(ON)} - V_{CE(sat)}}{R_B} = I_{RB}$$

Output low current $\equiv I_{OL}$

$$I_{OL} = I_{C,O(sat)} - I_{RC}$$

$$I_{RC} = \frac{V_{CC} - V_{CE,O(sat)}}{R_C}$$

$$I_{C,O(sat)} = \sigma_{OL} \beta_f I_{B,O(sat)}$$

* For maximum fan-out we consider operation at the edge of saturation where $\sigma = 1$

$$I_{C,O(sat)} = I_{C,O(EOS)} = \beta_f I_{B,O(EOS)}$$

$$I_{B,O} = I_{E,L} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,O(sat)}}{R_D}$$

* The emitter current of Q_L is found by analyzing the portion of the driver gate including V_{CC}, ρR_B, $(1-\rho)R_B$, Q_L, D_L, & Q_O as shown in figure to the right

* Considering Q_L & $(1-\rho)R_B$ as a super-node the current through ρR_B is equal to the emitter current of Q_L.

$$I_{E,L} = \frac{V_{CC} - V_{BE,L(FA)} - V_{D,L(ON)} - V_{BE,O(sat)}}{\rho R_B}$$

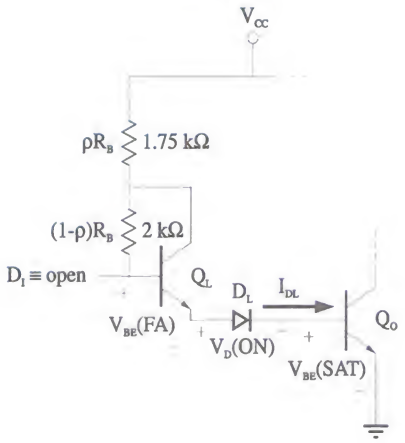


FIGURE 6.8 Portion of DTL Driving Gate for Fan-out Analysis and Power Dissipation Analysis

Example 6.2 ***DTL Fan-Out***

Calculate the fan-out for the DTL inverter of Figure 6.6 considering the circuit in Figure 6.7 and the sub-circuit in Figure 6.8. Let $\beta_F = 49$, $V_{BE}(FA) = 0.7$ V, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ V for the BJTs and $V_D(ON) = 0.7$ V for the diodes. Also, use $\alpha_{OL} = 0.85$ for the output low state.

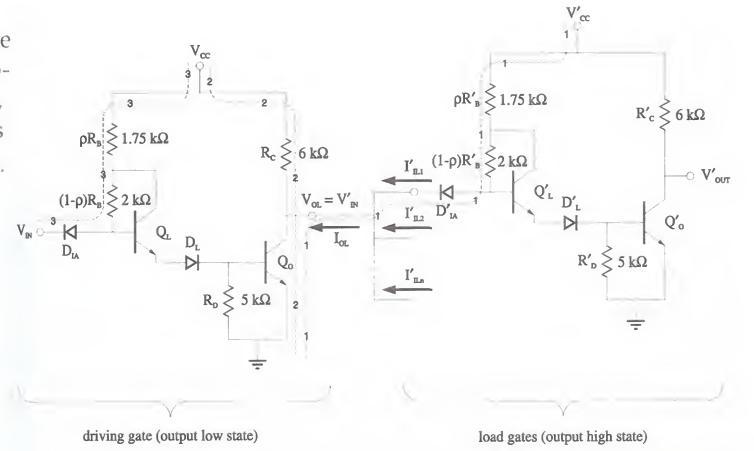


FIGURE 6.7 Cascaded DTL Gates for Fan-out and Power Dissipation Calculation

$$N = \frac{I_{OL}}{I_{IL}}$$

$$I_{IL} = \frac{V_{CC} - V_{D(ON)} - V_{CE(sat)}}{R_B}$$

$$= \frac{5 - 0.7 - 0.2}{3.75K} = 1.09\,mA$$

$$I_{OL} = I_{C,O}(sat) - I_{RC}$$

$$I_{RC} = \frac{V_{CC} - V_{CE,O}(sat)}{R_C}$$

$$= \frac{5 - 0.2}{6K\Omega} = 800\mu A$$

$$I_{C,O}(sat) = \alpha_{OL}\beta_F I_{B,O}(sat)$$

$$I_{B,O}(sat) = I_{E,L} - I_{RD}$$

$$I_{RD} = \frac{V_{BE,O}(sat)}{R_D} = \frac{0.8}{5K} = 160\mu A$$

For finding ρ

$$\frac{\rho R_B}{(1-\rho)R_B} = \frac{1.75K}{2K}$$

$$2\rho = 1.75 - 1.75\rho$$

$$3.75\rho = 1.75$$

$$\rho = \frac{1.75}{3.75} = 0.467$$

$$I_{E,L} = \frac{V_{CC} - V_{BE,L}(FA) - V_{DL}(ON) - V_{BE,O}(sat)}{\rho R_B} = \frac{5 - 0.7 - 0.7 - 0.8}{1.75K} = 1.60\,mA$$

$$I_{B,O}(sat) = 1.60m - 160\mu = 1.44\,mA$$

$$I_{C,O}(sat) = 0.85 \times 49 \times 1.44m = 60\,mA$$

$$I_{OL} = 60m - 800\mu = 59.2\,mA$$

$$N = \frac{59.2m}{1.09m} = 54.3$$

* The fan-out of this DTL gate is 54

DTL Power Dissipation

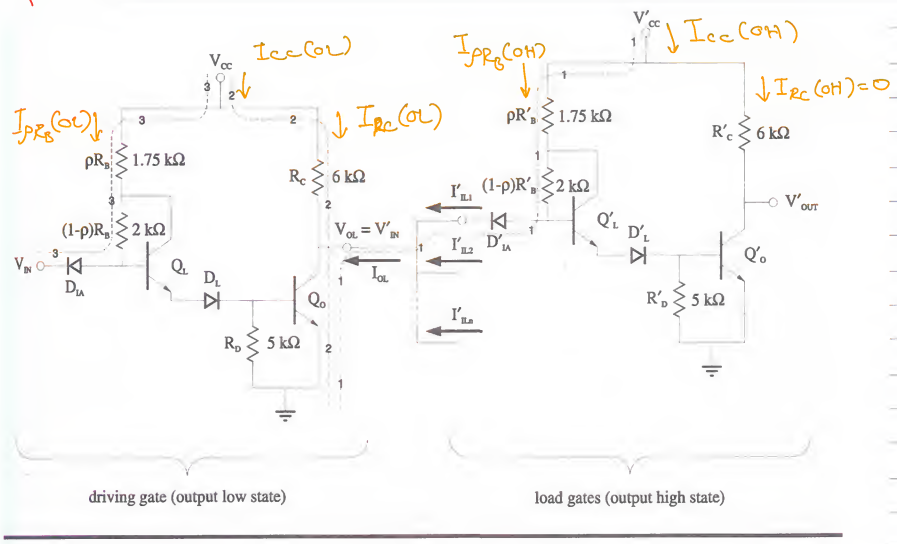


FIGURE 6.7 Cascaded DTL Gates for Fan-out and Power Dissipation Calculation

Output high current supplied $\equiv I_{CC(OH)}$

*For the output high state the input is low

$$I_{CC(OH)} = I_{\rho R_B(OH)} + I_{RC(OH)}$$

Since Q_o is cutoff $I_{RC(OH)} = 0$

$$I_{CC(OH)} = I_{\rho R_B(OH)} = I_{IL} = \frac{V_{CC} - V_{D(ON)} - V_{CE(sat)}}{R_B}$$

Output low current supplied $\equiv I_{CC(OL)}$

*For the low output state, the input is high

$$I_{CC(OL)} = I_{\rho R_B(OL)} + I_{RC(OL)}$$

$$I_{\rho R_B(OL)} = I_{E,L} = \frac{V_{CC} - V_{BE(FA)} - V_{D(ON)} - V_{BE(sat)}}{\rho R_B}$$

$$I_{RC(OL)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

Average power dissipation $\equiv P_{D(avg)}$

$$P_{D(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC}$$

$$= \frac{I_{\rho R_B(OH)} + I_{\rho R_B(OL)} + I_{RC(OL)}}{2} V_{CC}$$

Example 6.3 *DTL Power Dissipation*

Calculate the average power dissipation for the DTL gate in Example 6.2.

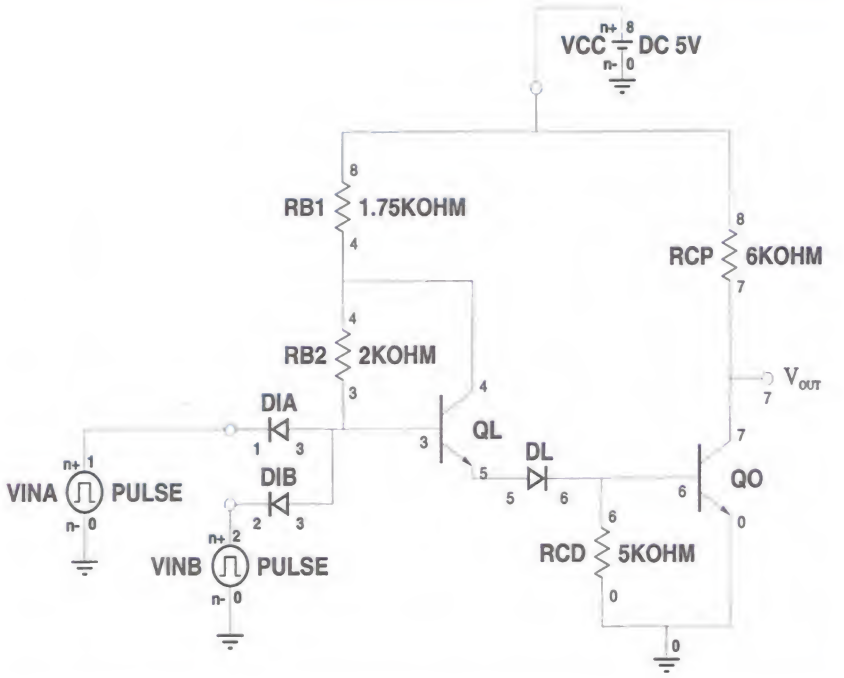
$$P_{D(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC}$$

$$= \frac{I_{pR_B(OH)} + I_{pR_B(OL)} + I_{RC(OL)}}{2} \cdot V_{CC}$$

$$= \frac{1.09m + 1.60m + 800\mu}{2} (5)$$

$$= 8.73\ mW$$

DTL SPICE Simulation



DTL Gate with SPICE Labelings

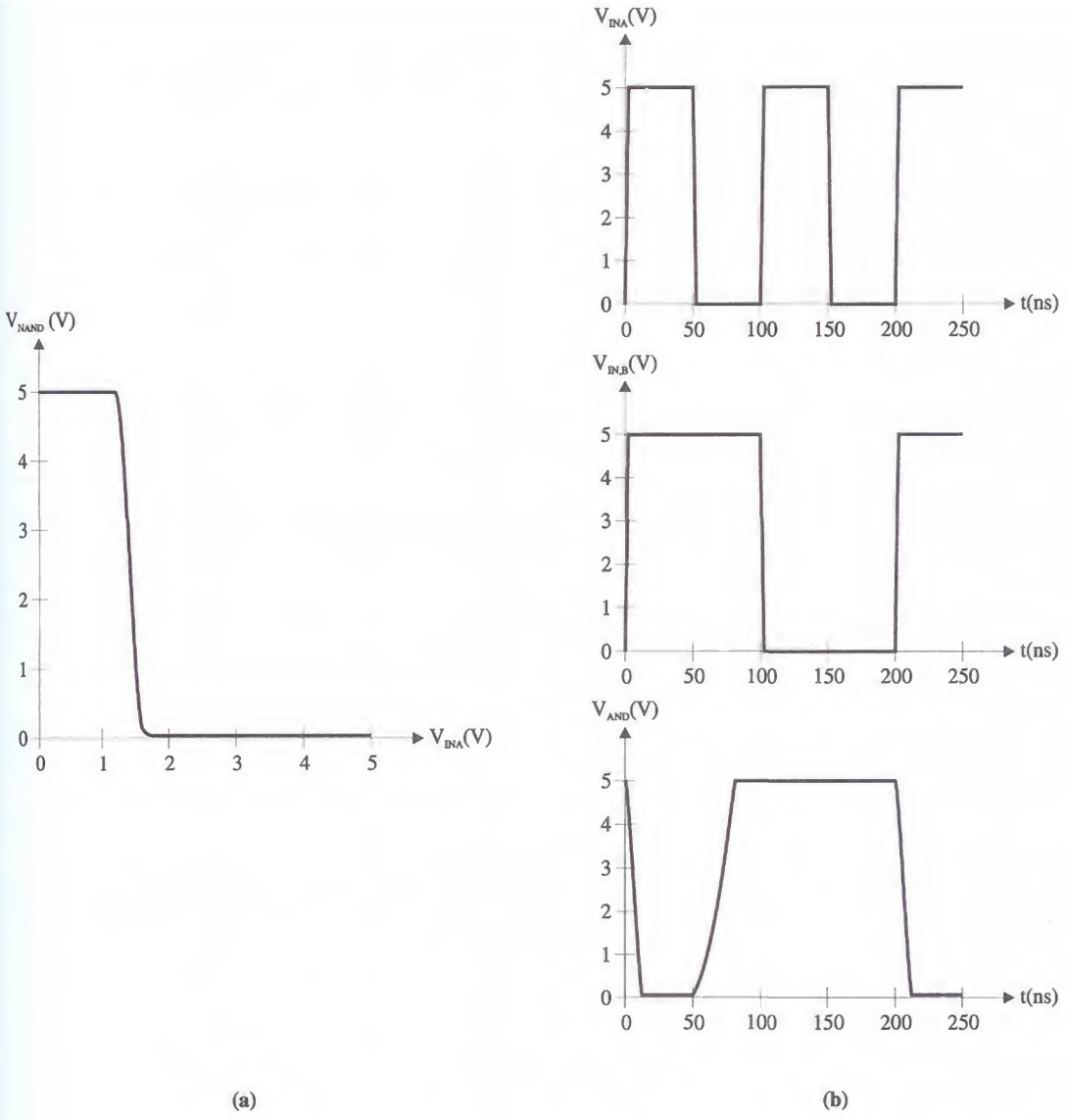


FIGURE 6.10 Results of Section 6.7 SPICE Simulation of DTL Gate: (a) Voltage transfer characteristic obtained from .DC sweep, (b) Transient response from .TRAN sweep